REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-5 and 7-31 are in the application. Claims 1, 15, 16, and 17, have been amended. Claim 6 previously was canceled. Dependent claims 28-31 have been added.

Specifically, claims 1, 15, and 16 have been amended to include, inter alia, features relating to the phase-variance device changing the duration of the switching-clock phases. Claim 17 now recites, inter alia, that there is a variable delay between the switching-clock phases

Dependent claim 28 contains the same feature as added to claim 1 herein, and dependent claims 29-31 each contain features similar to that in original claim 7.

In item 9 on page 5 of the above-identified Office Action, claims 17-21 and 24 have been rejected as being anticipated by Baschirotto et al. (U.S. 5,745,002) (herein "Baschirotto") under 35 U.S.C. § 102(b).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 4, lines 10-15 of the instant specification and is illustrated in Figs. 5B and 6B of the instant drawings.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 17 calls for, *inter alia*, a method for clocking successive operational amplifier stages constructed in switched op-amp technology, by:

generating at least two non-overlapping switching-clock signals;

switching a first operational amplifier on and off with a first signal of the two switching-clock signals;

switching a second operational amplifier on and off with a second signal of the switching-clock signals;

varying switching-clock phases of the first and second signals in which the operational amplifiers are switched off; and

providing a variable delay between the switching-clock phases of the first and second signals during which the operational amplifiers are switched off. (emphasis added)

The present invention relates to a circuit configuration in switched op-amp technology. A patentably distinguishing feature according to the present claims relates to enlarging or reducing the duration of the common off-phase of two non-overlapping signals when the detected switching speed of the transistors of the operational amplifiers is high or low, respectively. Such a circuit configuration or method has the advantage of fully exploiting at any time the power saving potential originating from fabrication and temperature variations.

Baschirotto discloses in column 7, line 62 to column 8, line 5 providing for **suitably delayed** clock phase signals, the delay being sufficiently large to suppress unwanted switching spikes when turning on operational amplifiers in a switched op-amp configuration. However, this disclosure does not suggest providing a **variable delay** within the circuit as recited in the instant claims. The disclosure in Baschirotto simply provides for a fixed, non-variable delay which is in any case (at least regarding, for example, temperature and fabrication variations) sufficiently large to suppress the unwanted

switching spikes. Applicants respectfully submit that the Examiner's analysis in item 5.9 of the above-identified Office Action is an overextended and incorrect interpretation of the wording "suitable delay" in the reference relying on improper hindsight reconstruction of Baschirotto in order to arrive at an on-chip implemented variable delay arrangement and method as recited in the instant claims.

Baschirotto discloses a low voltage switched capacitance circuit using switched operational amplifiers. The delay described in the reference is a delay of switching signals of the input signal (F1, F2 resp. to S3,S4) with respect to switching signals of the power supply of the operational amplifiers (F1a, F2a resp. A1, A2). The feature of "**providing a variable delay between the switching-clock phases of the first and second signals during which the operational amplifiers are switched off**" in claim 17 recites a variable delay between two switching signals for the power supply of two distinct operational amplifiers. Further, Baschirotto does not show or suggest introducing such a delay or phase variation. The phase variation is advantageous in that it reduces the time during which the operational amplifiers are turned on and therefore, reduces overall power consumption, which is not disclosed or obtained by the prior art reference.

Baschirotto does not show "providing a variable delay between the switching-clock phases of the first and second signals during which the operational amplifiers are switched off" as recited in claim 17 of the instant application.

Applicants also respectfully disagree with the Examiner's analysis under item 5.15 of the above-identified Office Action.

Baschirotto does not disclose introducing a variable delay between the first and second signal (i.e., between the signals which turn successive operational amplifiers on and off) as set forth in claim 17.

Baschirotto discloses corresponding signals $F1_a$ and $F2_a$ switching the operational amplifiers A1 and A2 shown in Fig. 5 and the corresponding description in the specification. Fig. 5 illustrates introducing some delay between the corresponding signals $F1_a$ and $F2_a$ switching operational amplifiers A1 and A2. This is, however, nothing more than what is already known in the prior art relating to switched op-amp technology.

As discussed previously by applicants, Baschirotto, in the relevant text in column 7, line 62 to column 8, line 5, fails to disclose any delay between the signals $F1_a$ and $F2_a$.

The text reads:

> "...in anticipating the turning on of A1 and... A2, as referred to the instant of connection.....of the switches(1) S2', S4 and S3.
>
> This may be ... implemented by driving the switches(2)... suitably delayed in respect to the homologous clock phase signal that turn on ... A1 and A2 and drive the switches S5 and S2'."

Thus, Baschirotto describes two groups of signals:

- the first group of (homologous) clock phase signals ($F1_a$ and $F2_a$) switches the operational amplifiers A1 and A2 and the switches S5 and S2' (see Fig. 4 and 5), and

- the second group of clock phase signals (F1 and F2) switches the switches S3, S4 and S6.

In the above-cited text, "the switches(1)" and "the switches(2)" refer to the same switches, namely the switches S3, S4 and S6 of the second group (erroneously S2' is cited in the text instead of S6, but the correct switch is readily apparent from Fig. 4).

Consequently, it is clear from the latter text that the

suitable delay is introduced between the first and second group of signals in order to suppress unwanted switching spikes. That text does not disclose a delay between the signals $F1_a$ and $F2_a$. As for the delay between the signals $F1_a$ and $F2_a$, the only relevant disclosure (namely, of providing a delay between these signals) is shown in Fig. 5. And Fig. 5 does not disclose a variable delay as recited in the claims of the instant application.

Baschirotto does not disclose anything for example about the size or the necessity of the delay between signals $F1_a$ and $F2_a$ and does not disclose anything about introducing any variable delay between these signals as set forth in claim 17.

Also, with respect to claim 21 which depends on independent claim 17, applicants disagree with the Examiner's analysis in item 14.1 of the above-identified Office Action, because no variation of any delay is disclosed by Baschirotto as discussed above relative to claim 17. Thus, in claim 21 the variation of the delay in dependence on the switching speed of transistors is not known nor shown or obvious from the prior art.

Baschirotto does not show "varying a duration of the switching-clock phases in which the operational amplifiers are

switched off dependent on a switching speed of transistors of the operational amplifiers" as recited in claim 21 of the instant application.

In item 17 on page 7 of the above-identified Office Action, claims 1-5, 7, 9-12, and 15-16 have been rejected as being unpatentable over Baschirotto in view of Saito (U.S. 5,723,998) and Fletcher (U.S. 6,392,466) under 35 U.S.C. § 103(a).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 7, lines 8-10 and page 24, lines 5-7 and 21-22 of the instant specification.

The foregoing discussion of Baschirotto is applicable in this rejection.

Saito discloses a detector for detecting the switching speed of transistors which is used as an estimate of the chip temperature.

Fletcher discloses a variation of clock signals using several independent controllable pulse-clock-delay apparatus on a

chip, each being associated with a particular functional block and outputting, based on an input clock signal, an appropriately varied pulse clock signal for the particular functional block. A given pulse-clock-delay apparatus controls, e.g., the operational mode of the associated functional block ("speed" or "race" condition path, see column 8, lines 47-48) in order to reduce processing delays or power consumption (see column 8, line 61).

Claim 1 is not obvious in view of Baschirotto, Saito, and Fletcher. Saito discloses varying the clock rate of an electronic circuit dependent upon the measured switching speed of the transistors but does not disclose varying the delay as recited in the instant claims. Fletcher discloses varying the delayed output clock signal in dependence of the intended operation mode of the associated functional block but does not give disclose anything about varying the delay as a function of detected parameters such as the switching speed of transistors. Further, Fletcher's teaching to generate a delayed output clock signal based on an input clock signal neither relates to the common off-phase of two clock signals nor to non-overlapping signals or switched op-amp technology in general as set forth in the claims of the instant application. And, as previously stated, Baschirotto does not disclose providing for a variable delay between two clock

signals in a switched op-amp technology.

Therefore, in the absence of hindsight, the feature of reducing or enlarging a variable delay between two non-overlapping clock signals in a switched op-romp configuration depending on the detected switching speed of transistors is neither shown nor is it suggested by the cited prior art.

The references do not show "a phase-variance device varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance device connected to said clock generator, said phase-variance device being configured for varying a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors as detected by said detector and enlarging said duration when said switching speed is high and reducing said duration when said switching speed is low" as recited in claim 1 of the instant application. Independent claims 15 and 16 contain similar limitations.

Moreover, the Examiner's analysis of dependent claim 7 set forth under item 23.2 of the above-identified Office Action is incorrect. Saito discloses to "measure the switching speed of the transistors constituting the processor" (see column 5,

lines 41-42), but does not disclose distinguishing between n- and p-channel transistors when detecting the switching speed of transistors as recited in dependent claim 7 of the instant application. Saito's approach for detecting switching speeds is to use chains of inverters (see Saito, Fig. 6, inverters 31-35 and Chiang, Fig. 1, inverters 12) or other logic gates (see Chiang, Fig. 2, AND gates 12'), whereby a single value is detected which depends on the switching speed of both n- and p-channel transistors. Therefore, the separate detection of the switching speeds of n- and p-channel transistors as claimed in dependent claim 7 is not disclosed nor rendered obvious by Saito or the other cited references.

The references do not show "said transistors include at least one of: n-channel FETs; and p-channel FETs; said transistors each have a respective switching speed; and said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs" as recited in dependent claim 7 of the instant application.

In item 30 on page 11 of the above-identified Office Action, claim 8 has been rejected as being unpatentable over Saito, Baschirotto, and Fletcher, and further in view of Chiang (U.S. 5,097,208) under 35 U.S.C. 103(a).

The foregoing discussion of Baschirotto, Fletcher, and Chiang apply equally in the rejection of claim 8 which depends on claim 1. Neither Fletcher nor Chiang overcome the deficiencies of Baschirotto.

Additionally, the references do not show a circuit "including an inverter chain, said detector having one of: an XOR gate with XOR inputs, one of said XOR inputs receiving an undelayed edge signal, and another of said XOR inputs receiving the edge signal delayed through said inverter chain; and an XNOR gate with XNOR inputs, one of said XNOR inputs receiving the edge signal and another of said XNOR inputs receiving the edge signal delayed through said inverter chain" as recited in dependent claim 8 of the instant application.

In item 34 on page 12 of the above-identified Office Action, claims 13-14 have been rejected as being unpatentable over Saito, Baschirotto and Fletcher and further in view of Larson (U.S. 4,951,303) under 35 U.S.C. § 103(a).

The previous discussion of Baschirotto and Fletcher apply equally in the rejection.

Larson discloses a high speed digital programmable frequency divider and does not overcome the deficiencies of the primary and secondary references.

Therefore, claims 13-14 are deeemed patentable over the cited prior art.

In item 39 on page 13 of the above-identified Office Action, claims 25-27 have been rejected as being unpatentable over Baschirotto and further in view of Saito under 35 U.S.C. § 103(a).

The previous discussions of Baschirotto and Saito are equally applicable in this rejection.

Claims 22-23 are therefore considered patentable over the cited references.

In item 41 on page 14 of the above-identified Office Action, claims 25-27 have been rejected as being unpatentable over Baschirotto and further in view of Larson under 35 U.S.C. § 103(a).

The previous discussions of Baschirotto and Larson are equally applicable in this rejection.

Claims 25-27 are therefore considered patentable over the cited references.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 15, 16, or 17. Claims 1, 15, 16, and 17, are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well, because they all are ultimately dependent on claim 1, 15, 16, or 17.

In view of the foregoing, reconsideration and allowance of claims 1-5 and 7-31 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

A check in the amount of $200.00 is enclosed herewith to cover the fee for the four additional dependent claims.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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FDP/bb

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